Stacked Device Enablement for Advanced Analog Design Simulations

Synopsys / Xilinx

ABSTRACT

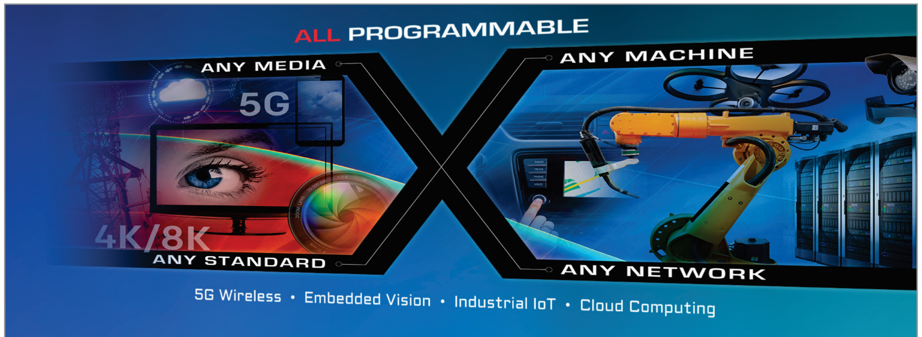
Advanced technologies such as FinFET with its excellent short channel control and higher performance/lower power has made it not only suitable for digital and SRAM scaling, but also for the applications in analog/RF design.

However the restriction of the design rules from the FinFET process poses chanleges to the analog design where an increasing need of multiple stacked transistors are used to realize a long-channel device. This has not only increased design complexity from schematic to simulation flow, but also the difficulty of getting the equivalent stacked device operating point and output characteristics.

To manage the challenge, we have collaborated with Synopsys and TSMC and developed a new design PDK flow and simulation methodology to handle the multiple serially connected transistors with a single stacked device macro.

The new stacked device with its enhanced SPICE simulation feature is presented in this talk. All the device parameters, such as operation point, threshold voltage and other analog/RF characteristics, can be obtained at the stacked device level in the same way as it does for individual transistors. The enhancement provids analog designers with a productive and accurate simulation tool to tackle the design complexity and challenge in advanced technology nodes.

An overview of the design simulation flow with the new stacked device feature will be presented using a 16nm FinFET design example.



XILINX ALL PROGRAMMABLE.

Stacked Device Enablement for Advanced Analog Design Simulations

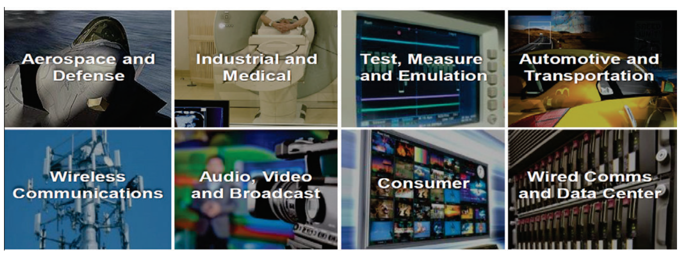
Susan Wu, Jane Xi, Jianlin Wei / *Xilinx Inc.*
HSPICE R&D / *Synopsys*

TSMC OIP, Sept. 13, 2017

Agenda

- Introduction
- Analog Design Challenge in Advanced Technology Nodes
- New Methodologies for Stacked Device Implementation in HSPICE
- Design Flow for the Stacked Device and Usage Examples
- Conclusions

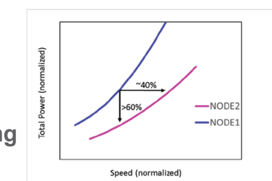
Xilinx: All Programmable



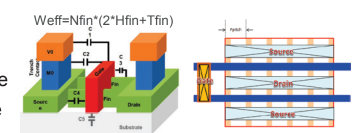
- Serving a wide range of diversified market
- Covering 'All' types of programmable devices – FPGA, SoC, MPSoC, and RFSoC
- Integrating 'all' types of technologies – logic, analog, CPU, and 3D-ICs
- Pioneering advanced technology initiatives with leading foundry TSMC and EDA partners

Advanced Technology Benefits and Its Challenges

- **Significant performance, power, area and cost improvement**
  - Substantially reduced short-channel effects
  - Reduced Vth → enables Lower Vcc, low power design
  - Faster performance, lower power



- **Enhanced analog gain and improved matching**
- **Challenges to analog design**
  - Quantized device sizes in FinFETs
  - Restricted design rules for channel length usage
  - Increased parasitic RC with 3D device structure

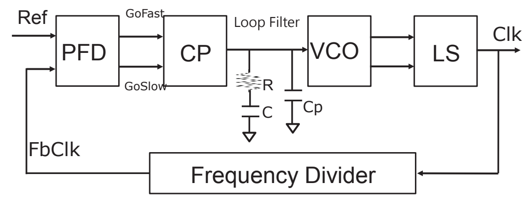


Xilinx Initiated Collaborations

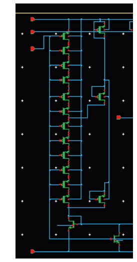
- **Decades of new methodology and EDA tools co-development for advanced technologies**
  - MOSRA for reliability (2006)
  - IVth for analog design output OP (2008)
  - 3D-IC for Multi-modules simulation in HSPICE (2012)

  Xilinx co-developed 3D-IC technology with TSMC (CoWoS), with the first 3D-IC FPGA in 2011
- **Stacked Device for analog design enablement in simulator/PDK**
  - This work in collaboration with EDA partners and TSMC
- **Early engagement and collaboration with EDA and foundry partners is imperative to the design success for a leading technology company**

A 16nm PLL Design Example



A PLL Circuit Block Diagram

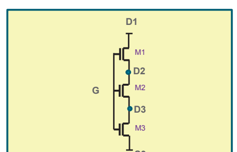


Stacked device usage

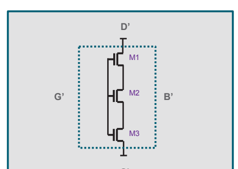
- Extensive stacked device usage in analog circuits such as VCO, Level Shifter and Charge Pump
- For better matching and noise margin

Methods for Stacked Device Analysis

- **A stacked device here refers to a serially connected transistors**
- **Traditional methods**
  - **Series connected transistors**
    - Only individual transistor characteristics can be obtained
  - **Subckt**
    - No direct reporting for OP (Operating Point), e.g. Vth, gm, etc.
    - Tedious work to set up measurement based on external nodal probing results
- **Enhanced SUBCKT Output Template in HSPICE**
  - SUBCKT OP characteristics can be obtained with proper setup
  - Maintain additional SUBCKT Library and some manual editing



Series connected transistors

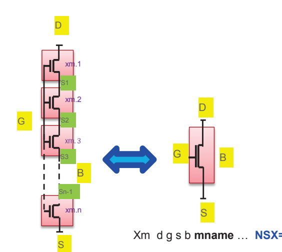


Subckt for Stacked device

New Stacked Macro Device Methodology

- **Use one primitive device to represent a series connected transistors**
  - Newly introduced instance parameter **NSX: Number of Stack**
  - Convenient and efficient to analog design,

    with NSX similar (reciprocal) to NF in SPICE model
- **Benefits**
  - Enables direct characterization of stacked device OP and major traditional transistor output templates
    - Vth, gm, gds, gmb, Vdmargin, Cgg, external nodal I & V, etc.
  - Support for DC, Transient, and AC analysis
  - An extended IVTH extraction method is defined
    - For accurate and efficient Vth and OP characterization



Expanded stacking devices Stacked macro device

IVTH Enhancement for Stacked Macro Device

- **IVTH syntax:**
  - **.IVTH model_name Ivth0=val DW=val DL=val VDSMIN=val DLSX=val**
  - X1 d g s b mname L=L0 W=W0 NF=NF0 **NSX=n** DLSX=value
- **The constant current for stacked macro device given as follows:**

$$Ivth = Ivth0 * \frac{W * SX\_factor + DW}{NSX*(L * SX\_factor + DL) + DLSX}$$

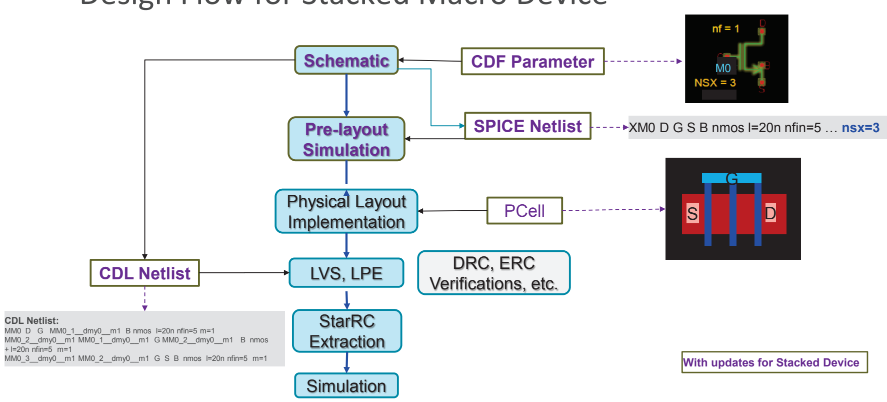
– .OPTION SX_factor=x (default 1.0): scale W/L for iVth definition.

Parameter	Description
Ivth0	Constant drain terminal current density
DW	Width offset for iVth current calculation
DL	Length offset for iVth current calculation
VDSMIN	User-defined minimum vds value
DLSX	Length offset for iVth stacked device current calculation

Stacked Macro Device Usage in HSPICE

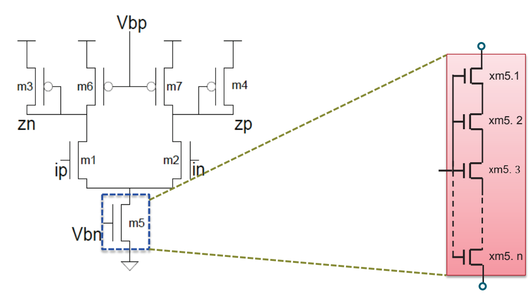
- A new control option “DEV_STACK” is added In HSPICE to enable stacked device netlist
- The feature of stacked device supports both subckt defined macro MOSFET (X element) and intrinsic MOS model defined transistor
- USAGE:
  - Syntax:
  - .option dev_stack=1
  - Xxxx nd ng ns nb subckt_name [other_options...] [NSX=val]
  - Mxxx nd ng ns nb mos_name [other_options...] [NSX=val]
  - .probe IVTH(Xxxx) IVTH(Mxxx) LX7(Xxxx) LX8(Mxxx)

Design Flow for Stacked Macro Device



The new design flow is transparent to the existing designs

Stacked Macro Devices Example - Schematic



- N-series connected transistors → **A single Stacked Device m5**
- **Much smaller, simpler schematic to maintain**
- **Critical parameters to check for stacked devices: Vth, Vd-margin, gm and Rout ... etc.**

Stacked Macro Device Examples – SPICE Netlist

- 6 stacked transistors netlisted in Stacked Macro Device format:

  XM5 d g s b nch   l='l0' nfin=nfin0 **nsx=6** multi=1 nf=1

- The Stacked Device elaborated in HSPICE:

```
XM5.xs_1  d   g s1 b  nch   nfin=nfin0 L=l0 nf=1
XM5.xs_2  s1 g s2 b  nch   nfin=nfin0 L=l0 nf=1
XM5.xs_3  s2 g s3 b  nch   nfin=nfin0 L=l0 nf=1
XM5.xs_4  s3 g s4 b  nch   nfin=nfin0 L=l0 nf=1
XM5.xs_5  s4 g s5 b  nch   nfin=nfin0 L=l0 nf=1
XM5.xs_6  s5 g s   b  nch   nfin=nfin0 L=l0 nf=1
```

Transparent to design

Stacked Device Netlist size is significantly reduced

Conclusion

- **New Stacked Device simulation methodology presented**
  - ✓ A productive and accurate simulation utility to tackle the increasing design complexity and challenge in advanced technology nodes
  - ✓ Simplified schematic, layout and SPICE netlist in design flow → benefit analog design
  - ✓ Enabled direct access to the stacked macro device characteristics as a single device
  - ✓ The new feature is available in the production release
- **The PDK flow enabled with the enhancement is transparent to users**
- **Close collaboration with leading EDA vendor and foundry partner is essential to the new design tool feature enablement**

Acknowledgment

- **Sincere thanks to Synopsys HSPICE team for support in enabling this feature in simulators, including Min Guo, Joddy Wang, Liping Zhu, etc.**
- **Special thanks to TSMC PDK and Model Teams, especially Jill Liu and Chung-Kai Lin for their valuable discussions and support**
- **Our appreciation also goes to Kuojim Huang and Xilinx CAD team for the design flow discussions and support**

Thank you

XILINX
ALL PROGRAMMABLE.